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ABSTRACT

Directly bonded ohmic InP/Si heterostructures are realized, overcoming the large (8%) lattice mismatch. By employing proper semiconductor surface pretreatments including cleaning and oxide removal, we obtain ohmic interfacial electrical characteristics at a bonding temperature as low as 200 °C. Among the doping-polarity combinations, ohmic interfacial electrical characteristics are observed for *n*-InP/*n*-Si and *n*-InP/*p*-Si bonded heterointerfaces, but not for *p*-InP/*p*-Si and *p*-InP/*n*-Si pairs. We numerically explain this polarity dependence in terms of energy band connections across the InP/Si heterointerfaces. The highly conductive III–V/Si direct bonding technique developed in this study is applicable for various heterostructured optoelectronic devices, such as multijunction solar cells and photonic integrated circuits.

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InP and its lattice-matched compounds are a promising semiconductor material family owing to their high carrier mobilities¹ and optical emission efficiencies^{2–5} for light-source applications and high photovoltaic efficiencies⁶ and radiation tolerance⁷ for solar-cell applications. However, such devices are composed primarily of III–V semiconductors, leading to high production costs. Si has advantages such as low cost, small weight, high mechanical strength, and high thermal conductivity. Therefore, Si is expected to improve the device performance and reduce the manufacturing cost by growing compound semiconductor solar cells, for example, on InP thin films bonded to Si substrates.⁸ In addition, InP/Si heterostructures can be used for hybrid photonic integrated circuits^{9,10} and high-efficiency multijunction solar cells. Therefore, the InP/Si heterostructure is promising for various optoelectronic applications.^{2–5,8,11} The most commonly used approach to fabricate semiconductor heterostructures is heteroepitaxial growth;^{12,13} however, the semiconductor combinations that can be used in the conventional heteroepitaxy are severely restricted by the lattice constant matching. The InP/Si heterostructure has a considerably large crystalline lattice mismatch of 8% between InP and Si, significantly larger than those of GaAs/Si (4%) and InP/GaAs (4%), which hinders the conventional heteroepitaxial growth. Alternatively, semiconductor wafer bonding is a promising scheme to fabricate high-crystalline-quality high-performance lattice-mismatched optoelectronic devices by overcoming the lattice matching restriction.^{14–16} Regarding InP/Si wafer bonding,^{2,4,5,8,11} only one study has been reported on an electrically conductive InP/Si interface,¹⁷ which presented data only of a single bonded sample; no systematic study on the

InP/Si electrical properties and analysis of conditions required to obtain a good conductivity has been reported. In this study, we fabricated InP/Si heterostructures by direct wafer bonding and investigated the interfacial conductivity in relation to material and process conditions.

We used a *p*-type InP wafer doped with zinc with a doping concentration of $5 \times 10^{18} \text{ cm}^{-3}$, an *n*-type InP wafer doped with sulfur with a doping concentration of $7 \times 10^{18} \text{ cm}^{-3}$, a *p*-type Si wafer doped with boron with a doping concentration of $2 \times 10^{19} \text{ cm}^{-3}$, and an *n*-type Si wafer doped with phosphorus with a doping concentration of $2 \times 10^{19} \text{ cm}^{-3}$. All the used wafers were epi-ready-grade single-side-polished wafers. The polished surface of each wafer was coated using a photoresist film to protect the bonding surface during the dicing process. The Si and InP wafers were then diced into $\sim 1 \text{ cm}^2$ pieces. The diced wafers were submerged in acetone for 5 min to remove the photoresist film and degrease the bonding surfaces. We carried out an SC-1 surface cleaning ($\text{NH}_3:\text{H}_2\text{O}_2:\text{H}_2\text{O} = 13:17:70 \text{ wt:wt:wt}$) and HFAq (10 wt. %) surface treatments for 10 and 1 min, respectively, to remove particles and native surface oxide.¹⁸ Such a HF treatment is commonly carried out in device fabrication processes for InP-related materials.^{18–20} However, it is known that the InP surface exhibits rapid reoxidation upon air exposure.²¹ Therefore, the Si and InP surfaces were then brought into contact with each other in the HFAq. In this manner, the polished sides of Si and InP piece surfaces came into contact with each other and bonded under a uniaxial pressure of 0.1 MPa G at various temperatures in the range of 100–500 °C in ambient air for 3 h. The heating and cooling rates were around 10 °C/min. For

electrical measurements, metal electrodes comprising an Au–Ge–Ni alloy (80:10:10 wt:wt:wt) and pure Au with thicknesses of 30 and 150 nm were sequentially deposited by thermal evaporation to both outer sides of the bonded InP/Si pieces, respectively. In this manner, Au/Au–Ge–Ni/InP and Au/Au–Ge–Ni/Si contacts were formed, covering the entire InP and Si surfaces of the bonded samples. We did not apply any annealing for the contacts to prevent potential heating influences to the bonded interfacial characteristics. In addition, detaching normal stresses were measured for the bonded samples to represent the bonded interfacial mechanical strength.

At all the tested bonding temperatures, InP/Si bonding was formed. Figure 1 shows a typical cross-sectional scanning electron microscopy image of the directly bonded InP/Si heterointerface. The wafers have a firm and uniform contact with each other with a mechanical stability sufficient to endure the cleavage of the bonded-pair sample. Incidentally, atomic-scale investigations for directly bonded InP/Si interfaces have been carried out using transmission electron microscopy in earlier studies.^{11,17,20} Figure 2 shows typical current–voltage characteristics of the samples with bonded *n*-type InP/*p*-type Si heterointerfaces at various bonding temperatures. We obtained InP/Si heterointerfaces with ohmic electrical characteristics for bonding temperatures equal to and higher than 200 °C. For Si/Si hydrophobic direct wafer bonding, for example, it is thought that annealing provides an increase in the hydrogen bonds and further covalent bond formation via HF and hydrogen release,^{22–24} and a drastic increase in the bonding interfacial energy was observed around an annealing temperature of 150 °C.²⁴ For heterointerfaces formed by direct wafer bonding of dissimilar semiconductors such as InP/Si,²⁵ Ge/Si,²⁶ and GaAs/InP^{27,28} systems, there thought to be additional annealing effects of atomic interdiffusion and recrystallization of interfacial amorphous regions. The ohmic bonding interface formation at 200 °C or above can thus be attributed to such heat-induced interfacial evolutions that enhance the interfacial electrical conductance. Such a low bonding temperature is safe so as to not degrade any semiconductor material component, including even delicate nanostructures such as quantum wells and dots; it is also effective to ensure low process costs in device production. In order to statistically investigate the

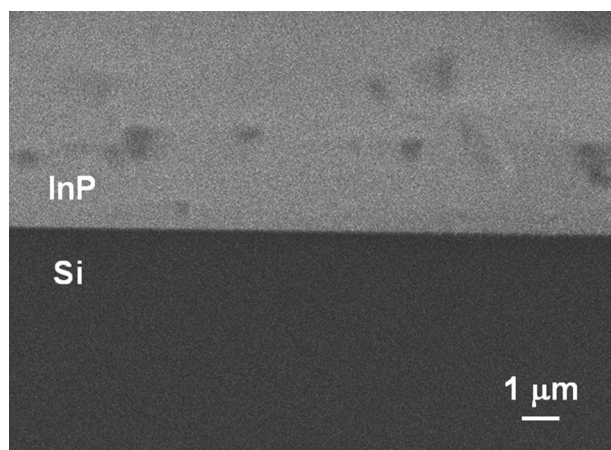


FIG. 1. Cross-sectional scanning electron microscopy image of the bonded InP/Si heterointerface.

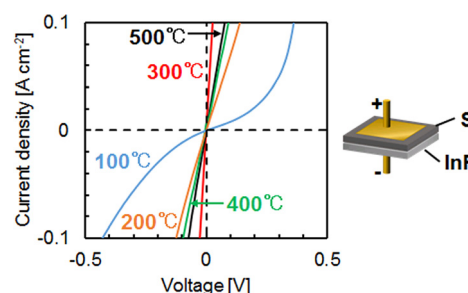


FIG. 2. Current–voltage characteristics of the samples with bonded *n*-InP/*p*-Si heterointerfaces at various bonding temperatures.

tendency of the interfacial electrical conductance depending on the bonding temperature, Figs. 3(a) and 3(b) show the electrical resistivities and mechanical strengths, respectively, of the samples with bonded InP/Si heterointerfaces at various bonding temperatures for all the bonded samples fabricated in this study. It is worth noting that each of the presented resistivities is derived by determining the slope of the tangential line of the current–voltage curve at an applied bias voltage of 0 V. The obtained statistics in Fig. 3 does not show a monotonous behavior, attributed to the trade-off between the conductivity increase and decrease by the formation of covalent bonds and the thermal expansion mismatch between InP and Si at higher temperatures. Interfacial oxide formation might also be the origin of higher interfacial resistivities at higher temperatures for our wafer bonding process in ambient air.^{17,21} It should also be noted that the wafer bonding process leads to some randomness in the reproducibility of the bonded sample interfacial properties, degradable even by a single-particle accidental incorporation into the interface. However, our results show a general tendency that the interfacial electrical conductivity and reproducibility increase with the bonding temperature; particularly, high-reproducibility low-resistivity interfaces are obtained at temperatures equal to and higher than 300 °C. Therefore, we chose 300 °C as the bonding temperature for the following experimental investigations with other doping-polarity combinations.

Figure 4 shows the dependences of the current–voltage characteristics of the samples with bonded (at 300 °C) InP/Si heterointerfaces on the doping-polarity (*p*-type or *n*-type) combinations. We obtained ohmic interfacial electrical characteristics at the InP/Si heterointerfaces for the doping-polarity combinations of *p*-type Si/*n*-type InP and *n*-type Si/*n*-type InP, while rectified diode-like characteristics were obtained for *p*-type Si/*p*-type InP and *n*-type Si/*p*-type InP. In order to

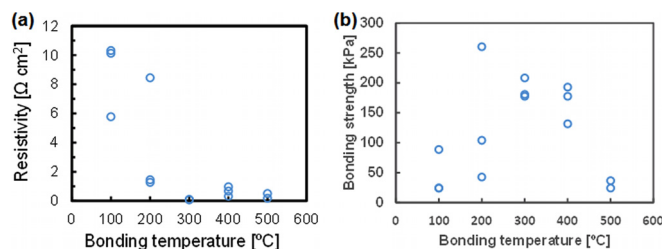


FIG. 3. Statistics of (a) electrical resistivities and (b) mechanical strengths of the samples with bonded *n*-InP/*p*-Si heterointerfaces at various bonding temperatures.

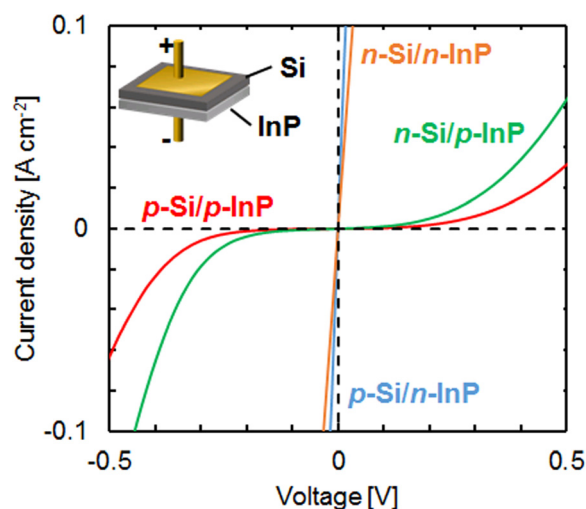


FIG. 4. Current-voltage characteristics of the samples with bonded InP/Si heterointerfaces (bonding temperature: 300 °C) with various doping-polarity combinations.

explain this polarity-dependent behavior, we analyzed the energy-level connections at the InP/Si heterointerfaces. Figure 5 shows the energy-level profiles of the conduction and valence band edges across the InP/Si heterointerfaces with varying doping polarities and concentrations, calculated by one-dimensional simulations of heterojunction band bending (PC1D software, University of New South Wales). We set the doping concentrations of each semiconductor material in this calculation equal to those in the Si and InP wafers used for the bonding experiments. These results indicate that for the homo-polarity combinations, i.e., *p*-type Si/*p*-type InP and *n*-type Si/*n*-type InP, the thinner potential barrier at the valence band edge for the *n*-type/*n*-type combination than the *p*-type/*p*-type combination [Figs. 5(a) and 5(b)] can be

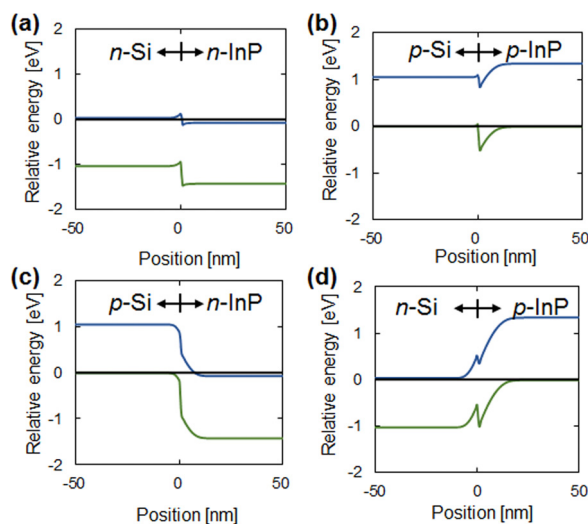


FIG. 5. Calculated profiles of the conduction and valence edges across the InP/Si heterointerfaces with various doping polarities and doping concentrations used in the experiments.

the origin of the higher interfacial electrical conductivity and ohmic characteristics across the InP/Si heterointerface. On the other hand, for the hetero-polarity combinations, i.e., *n*-type Si/*p*-type InP and *p*-type Si/*n*-type InP, the smaller distance between the valence and conduction band edges across the InP/Si heterojunction for the *p*-Si/*n*-InP combination than the *n*-Si/*p*-InP combination [Figs. 5(c) and 5(d)] may enable tunneling carrier transport, leading to a higher conductivity.

It should be noted that the current-voltage data in Fig. 4 include all the series resistances through the samples. Therefore, we independently determined the contact resistance of the metal electrode/semiconductor interface by the transmission line method and then determined the nominal resistivity at the bonded interface by subtracting it from the slope of the current-voltage curve in Fig. 4. The determined interfacial electrical resistivities of *n*-type InP/*p*-type Si and *n*-type InP/*n*-type Si were 0.048 and 0.19 Ω cm², respectively. Therefore, a set of favorable electrical interlayer conductances was obtained in the fabricated InP/Si heterostructures, suitable for various optoelectronic applications. For example, for photovoltaic applications, the InP/Si direct bonding technology developed in this study may enable realization of ultrahigh-efficiency lattice-mismatched multijunction solar cells comprising InP- and Si-based subcell sets, such as an AlAsSb/AlInAs/InP/Si/SiGe five-junction cell. Furthermore, any combination of GaAs-, InP-, and Si-based subcells could be flexibly realized as GaAs/InP^{29,30} and GaAs/Si^{31,32} direct bonding technologies have already been established.

In this study, we investigated the InP/Si direct wafer bonding focusing on the interfacial electrical conductance. Ohmic low-resistivity InP/Si heterointerfaces were obtained, overcoming the crystalline lattice mismatch of 8%, by choosing proper sets of surface treatments and process conditions. Furthermore, the ohmic heterojunction was fabricated at a low bonding temperature of 200 °C, which is safe not to degrade any semiconductor structure and effective for production cost reduction. In addition, the dependence of the electrical conductivity on the doping-polarity combination was explained through heterointerfacial energy band calculations. The InP/Si directly bonded heterostructures developed in this study pave the way for the realization of high-performance optoelectronic devices.

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